WHAT IS CLAIMED IS:

1. A method for optimizing clock distribution in a circuit to reduce the effect of power supply noise comprising:

determining a response curve of a power source for a circuit;

determining a delay sensitivity of a clock net in the circuit to the power source;

determining a delay sensitivity of a data net in the circuit to the power source;

determining a data delay for the data net;

determining a clock delay for the clock net; and

adjusting the clock delay to reduce the effect of power supply noise on the data net, the adjusting being based on the response curve of the power source, the delay sensitivity of the clock net, the delay sensitivity of the data net, the data delay, and the clock delay.

2. The method according to claim 1, further comprising defining a clock frequency of the circuit; and using the clock frequency in determining the adjusting.

3. The method according to claim 1, further comprising adjusting the clock delay by adding a pre-distribution clock delay based on the response curve of the power source, the sensitivity of the clock net, the sensitivity of the data net, the data delay, and the clock delay.

4. The method according to claim 3, further comprising determining a delay of the pre-distribution clock delay net, determining a sensitivity of the pre-distribution clock delay net, and basing the adjusting on the delay of the pre-distribution clock delay net and the sensitivity of the pre-distribution clock delay net.

5. The method according to claim 3, further comprising adding the pre-distribution clock delay at the beginning of a clock distribution tree that includes the clock net.

6. The method according to claim 1, further comprising performing the first determining step through the fifth determining step using a simulator.

7. The method according to claim 6, further comprising performing the first determining step through the fifth determining step using a MATLAB simulator.

8. A circuit on a die for optimization of clock delay to minimize the effect of power supply noise comprising:

a clock generator;

a clock tree comprising a plurality of clock nets;

at least one delay element connected between the clock generator and the clock tree, the at least one delay element delaying a clock signal from the clock generator to the clock tree; and

at least two storage devices, the at least two storage devices storing data received upon receipt of the clock signal,

wherein the delay caused by the at least one delay element is set to provide a delay of the clock signal that minimizes the effect of noise from a power source on the clock signal as it travels along the clock nets and on the data as it travels along a data path between two of the at least two storage devices.

9. The circuit according to claim 8, wherein the clock generator comprises a phase locked loop (PLL) device.

10. The circuit according to claim 8, wherein the at least one delay element comprises at least one of a transistor, a logic gate, and a Field Effect Transistor (FET).

11. The circuit according to claim 8, wherein the at least two storage devices comprise latches.

12. The circuit according to claim 8, wherein the delay caused by the at least one delay element is set based on the delay and sensitivity of the clock nets, the delay and sensitivity of the data paths, and a transient voltage droop curve for the power supply.

13. A circuit on a die for optimization of clock delay to minimize the effect of power supply noise comprising:

a clock generator;

a clock tree comprising a plurality of clock nets;

at least two storage devices, the at least two storage devices storing data received upon receipt of a clock signal from the clock generator; and

at least one filter element connected between a power source and at least one element transferring the clock signal in the plurality of clock nets, the at least one filter element filtering noise from the power source.

14. The circuit according to claim 13, wherein the clock generator comprises a phase locked loop (PLL) device.

15. The circuit according to claim 13, wherein the at least two storage devices comprise latches.

16. The circuit according to claim 13, wherein the design of the filter is based on the delay and sensitivity of the clock nets, the delay and sensitivity of the data paths, and a transient voltage droop curve for the power source.

17. A processor microcircuit comprising:

a clock generator;

a clock tree comprising a plurality of clock nets;

at least one delay element connected between the clock generator and the clock tree, the at least one delay element delaying a clock signal from the clock generator to the clock tree; and

at least two storage devices, the at least two storage devices storing data received upon receipt of the clock signal,

wherein the delay caused by the at least one delay element is set to provide a delay of the clock signal that minimizes the effect of noise from a power source on the clock signal as it travels along the clock nets and on the data as it travels along a data path between two of the at least two storage devices.

18. The processor according to claim 17, wherein the clock generator comprises a phase locked loop (PLL) device.

19. The processor according to claim 17, wherein the at least one delay element comprises at least one of a transistor, a logic gate, and a Field Effect Transistor (FET).

20. The processor according to claim 17, wherein the at least two storage devices comprise latches.

21. The processor according to claim 17, wherein the delay caused by the at least one delay element is set based on the delay and sensitivity of the clock nets, the delay and sensitivity of the data paths, and a transient voltage droop curve for the power supply.

22. A method for optimizing clock distribution in a circuit to reduce the effect of power supply noise comprising:

determining a transient curve for a power supply voltage droop, a delay and sensitivity of a pre-distribution, a delay and sensitivity of a clock distribution for a clock signal, and a delay and sensitivity of a data path, the clock signal comprising a plurality of clock pulses;

deriving normalized sensitivity curves for the pre-distribution, the clock distribution, and the data path;

computing the delay error due to propagation of generation clock edge through the pre-distribution and the clock distribution by integrating the normalized sensitivity curve for pre-distribution and the normalized sensitivity curve for the clock distribution for each clock pulse;

computing the delay modulation for the data path by integrating the normalized sensitivity curve for the data path at a first clock pulse, the first clock pulse representing when the power supply voltage droop begins;

computing the delay error due to propagation of sampling clock edge through the pre-distribution and the clock distribution by integrating the normalized sensitivity curve for the pre-distribution and the normalized sensitivity curve for the clock distribution;

computing the net timing loss for the first clock pulse by summing the integrals resulting from the first computing step, the second computing step, and the third computing step; and

repeating all computing steps for each successive clock pulse until a desired number of clock pulses have been completed.

23. The method according to claim 22, further comprising constructing a net timing loss curve to identify a maximum timing loss.

24. The method according to claim 23, further comprising revising at least one of the pre-distribution delay and the pre-distribution sensitivity based on the maximum timing loss.